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06EC45

Fourth Semester B.E. Degree Examination, June/July 2014
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. What are different types of ports in VHDL and verilogs? Explain them briefly. **(05 Marks)**

b. What are the different types of VHDL data types? Explain them with examples. **(10 Marks)**

c. Explain the comparison between VHDL and verilogs. **(05 Marks)**

2 a. Write verilog code for 2 × 2 bit unsigned combinational array multiplier, also write its gate level diagram. **(06 Marks)**

b. Write VHDL code for 3 bit ripple carry adder using data flow description. **(08 Marks)**

c. Explain the features of data flow style of description with an example. **(06 Marks)**

3 a. Write verilog code for bahavioural descriptions of a 2 × 1 MUX with tristate o/p using ELSE-IF. **(06 Marks)**

b. Illustrate the difference between signal and veriable assignment statements in VHDL code by writing behavioral description of a D-latch. Also write its simulation waveform. **(08 Marks)**

c. Explain the different types of loop statements in VHDL and verilog. **(06 Marks)**

4 a. What is binding? How binding between entity and architecture in VHDL and binding between two modules in verilog is achieved? Explain with examples. **(08 Marks)**

b. Write VHDL structural description of a pulse triggered Master-Slave JKFF using a Master-Slave D-flip-flop. **(08 Marks)**

c. What are the highlights of structural description? **(04 Marks)**

PART – B

5 a. What are procedures and tasks in HDL? Explain them with examples. **(08 Marks)**

b. Write verilog code for converting an unsigned binary number to an integer using task, also write simulation o/p for conversion. **(06 Marks)**

c. Write VHDL code to find the greater of two signed numbers using function. **(06 Marks)**

6 a. Write a note on VHDL packages? Explain with examples. **(06 Marks)**

b. Write VHDL code for addition of two 5 × 5 matrics using package, considering the numbers for matrices. Write its result. **(06 Marks)**

c. With a block diagram and functional table, write VHDL code for 16 × 8 SRAM. **(08 Marks)**

7 a. What are highlights of mixed language description? With an examples show how to invoke a verilog module from a VHDL module. **(08 Marks)**

b. Write mixed language description for Full adder using two half adders with invoking a VHDL entity from a verilog module. **(06 Marks)**

c. Write mixed language description for a 4 bit priority encoder using CASEX in VHDL. Write its truth table. **(06 Marks)**

8 a. Define synthesis. With a flow chart, explain the steps in a general synthesis process. **(08 Marks)**

b. Explain verilog synthesis information from module inputs/outputs with examples. **(06 Marks)**

c. Write a note on mapping logical operation. Write VHDL and verilog code. Draw its logic symbol and gate level logic diagram. **(06 Marks)**

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